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The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE



BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES



Ex parte HAJIME AKIMOTO, MITSURU HIRAKI, HITOSHI NAKAHARA, TAKASHI AKIOKA, YOSHIYUKI KANEKO, MAKOTO TSUMURA, and YOSHIRO MIKAMI

Appeal No. 2003-1663
Application 09/975,934[1]

HEARD: January 6, 2004

Before BARRETT, BARRY, and SAADAT, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-15.

We affirm.

[1] Application for patent filed October 15, 2001, entitled "Image Display Device," which is a continuation of Application 09/043,534, filed March 20, 1998, now U.S. Patent 6,329,973, issued December 11, 2001, which is a national stage application under 35 U.S.C. § 371 of PCT Application PCT/JP95/01886, filed September 20, 1995.

## BACKGROUND

The invention relates to an image display.

Claim 1 is reproduced below.

> 1. An image display which displays image data on an image display part constructed by a display pixel array, wherein an image data input circuit inputs image data into the image display part by selecting addresses in a row direction and a column direction of the display pixel array so that the display pixel array has two neighboring areas having different frame rates (>0);
>
> wherein the display pixel array includes row direction address lines and column direction address lines; and
>
> wherein display pixels of the display pixel array each include an AND functional circuit which is connected to one of the row direction address lines and one of the column direction address lines.

No references are relied upon in the rejection.

Claims 1-15 stand rejected under 35 U.S.C. § 101 as claiming the same invention as that of claims 1-9 and 11-16, respectively, of appellants' U.S. Patent 6,329,973 ('973 patent), which issued from parent Application 09/043,534 of the present application.

We refer to the final rejection (Paper No. 6) and the examiner's answer (Paper No. 13) (pages referred to as "EA__") for a statement of the examiner's rejection, and to the brief (Paper No. 11) (pages referred to as "Br__") and reply brief (Paper No. 14) (pages referred to as "RBr__") for a statement of appellants' arguments thereagainst.

OPINION

Same-invention double patenting under 35 U.S.C. § 101 means identical subject matter. In re Vogel, 422 F.2d 438, 441, 164 USPQ 619, 621 (CCPA 1970). "A good test, and probably the only objective test, for 'same invention,' is whether one of the claims could be literally infringed without literally infringing the other. If it could be, the claims do not define identically the same invention." Id. at 441, 164 USPQ at 622. Same-invention double patenting cannot be overcome by filing a terminal disclaimer.

Claims 1-15 of the present application are identical to claims 1-9 and 11-16, respectively, of the '973 patent, except that independent claims 1, 10, 14, and 15 of the present application recite an "AND functional circuit" whereas claims 1, 11, 15, and 16, respectively, of the '973 patent recite an "AND logical circuit." The AND circuit is described in connection with the pixel array in Fig. 2. The pixel array contains an AND gate circuit 47 for driving the gate of the TFT switch 48, the AND gate formed by a CMOS process, where the input terminals of the AND gate circuit 47 are connected to a vertical direction gate selection line 50 and a horizontal direction gate selection line 46 in the row and column directions, respectively (specification, p. 8, line 19 to p. 9, line 4).

The examiner finds that the "AND functional circuit" of the present application and the "AND logical circuit" of the '973 patent are directed to the same AND gate circuit and, therefore, are claiming the same invention (EA3).

Appellants argue that the proper test is whether the application claims claim the same invention as the patent claims, not whether they read on the same element (Br6-7; Br11-12).

We agree with appellants that the test for same-invention double patenting is whether the application claims claim the same invention as the '973 patent claims. The fact that the claims read on the same element does prove that the scope is identical. Therefore, we must examine the scope of the claims.

Appellants argue that the term "AND functional circuit" in the application claims is broader than the term "AND logical circuit" recited in the patent claims, such that there are embodiments of the invention which fall within the scope of the application claims but do not fall within the scope of the patent claims (Br6-7). Appellants refer to the statement in Taub and Schilling, Digital Integrated Electronics (McGraw-Hill 1977), p. 440, "[i]n logical gates all inputs and outputs are digital signals," and argue that one of ordinary skill in the art might arguably interpret "AND logical circuit" to mean a logical circuit which performs an AND function and is implemented with a digital circuit (Br7-8; RBr4). It is argued that the AND circuit

is not limited to implementation with a digital circuit, but would include implementation with an analog circuit (Br8; RBr4). To compensate for the possibility that the scope of independent claims 1, 11, 15, and 16 of the '973 patent might be unduly limited by an arguable interpretation of the "AND logical circuit" as being implemented by a digital circuit, independent claims 1, 10, 14, and 15 of the present application recite an "AND functional circuit," which, it is argued, one of ordinary skill in the art would understand is not limited to implementation with a digital circuit, but means any circuit which performs an AND function, implemented with either a digital circuit or an analog circuit (Br8; RBr4-5; RBr8). Thus, it is argued, the claimed inventions are not identical because the "AND functional circuit" of the present invention includes an analog circuit which performs an AND function, but an analog circuit would arguably not fall within the scope of the "AND logical circuit" of the claims of the '973 patent (Br8; Br12; RBr8-9).

We conclude that the terms "AND functional circuit" in the present application and "AND logical circuit" in the '973 patent are synonyms for the exact same thing and, thus, the scopes of the claims are identical. An "AND circuit" is any circuit which performs the Boolean logic function that when all the inputs are a logical "true" (conventionally represented as "1"), the output is a logical "true" ("1"), and when one or more inputs are a

logical "false" (conventionally represented as "0"), the output is a logical "false" ("0"). An "AND" operation is, by definition, a "logical" operation, so "AND logical" to describe a circuit is redundant. An "AND" operation is also, by definition, a function, so "AND functional" to describe a circuit is redundant. The terms "AND circuit," "AND logical circuit," "AND functional circuit," and "AND logical functional circuit" all have the same meaning. An "AND" operation necessarily implies operation with digital signals, i.e., signals that represent either a "1" or a "0." An analog circuit which performs an AND function has to be operating using digital logic signals, i.e., with signals that the circuit interprets as "1" or "0"; it does not make sense to define an "AND" operation in terms of analog (continuous) signals. The statement in Digital Integrated Electronics that "[i]n logical gates all inputs and outputs are digital signals," only refers to the digital data representation and does not imply anything about the implementation of the logic circuits. Appellants may be confusing digital signals with the circuitry that implements the signals. While there are some logic implementations that could be considered pure digital (e.g., a switch which is either closed or open), there are many logic implementations that use analog devices to produce signals that the circuit interprets as digital signals (e.g., transistors). Any circuit which performs an AND function is an

"AND circuit," an "AND logical circuit," and an "AND functional circuit." We conclude that the terms "AND functional circuit" in the present application and "AND logical circuit" in the '973 patent are semantically equivalent and, thus, are identical in scope. The rejection of claims 1-15 for same-invention double patenting under 35 U.S.C. § 101 is sustained.

The examiner's other reasoning (EA4), and appellants' response thereto (RBr6-9), does not affect the analysis.

CONCLUSION

The rejection of claims 1-15 under 35 U.S.C. § 101 for same-invention double patenting is sustained.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

LEE E. BARRETT
Administrative Patent Judge )

LANCE LEONARD BARRY
Administrative Patent Judge ) BOARD OF PATENT APPEALS AND INTERFERENCES

MAHSHID D. SAADAT
Administrative Patent Judge )

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